REMARKS

I. Introduction

Claims 1-36 are pending in this application, of which claim 1 is independent. In this Amendment, claim 1 has been amended. Care has been exercised to avoid the introduction of new matter. Support for the amendment of claim 1 can be found in, for example, on page 4, lines 9-17 of the specification.

II. The Rejection of Claims 1-36 under 35 U.S.C. §112, Second Paragraph

The Examiner asserted, "[i]t is unclear what it means for the frequency error to be 'great'" (paragraph 3 of the Office Action). In this amendment, claim 1 has been amended. Applicants believe the amendment to the claim is fully responsive to the Examiner's concerns. Withdrawal of the rejection of the claims is, therefore, respectively solicited.

III. The Rejection of Claims 1-5 and 18 under 35 U.S.C. §102

Claims 1-5 and 18 have been rejected under 35 U.S.C. §102(b) as being anticipated by Hamada et al. In the statement of the rejection, the Examiner asserted that Hamada et al. discloses a clock adjusting device which identically corresponds to the claimed subject matter.

Applicants emphasize that there is a difference between the claimed subject matter and the device of Hamada et al. in that the claimed subject matter is directed to elimination of a phase error amount due to a frequency error, whereas Hamada et al. is directed to detection of a phase error amount of a reproduction signal.

Hamada et al. discloses accurately detecting a phase error amount of a reproduction signal even when an offset amount is superimposed in the reproduction signal, as well as when no offset amount is superimposed in the reproduction signal. In Hamada et al., a sample value of

the reproduction signal is obtained on the basis of a predetermined reference level, an offset amount is calculated, and then, the reference level is adjusted based on the offset amount (the calculated offset amount is deducted from the sample value of the reproduction signal obtained based on the reference level, in case of no offset amount), in order to accurately detect a phase error amount of the reproduction signal.

On the other hand, the claimed subject matter addresses a problem appears when a synchronous clock which is synchronized with reproduced data is not extracted and the reproduced data is sampled by a sampling clock (i.e., a not-yet-synchronized clock) which is not yet adjusted to have a frequency of the synchronous clock (i.e., there is a frequency error between the synchronous clock and the not-yet-synchronized clock). In that case, the reproduced data sampled by the not-yet-synchronized clock has a value different from reproduced data sampled by the synchronous clock, meaning that there is an phase error amount resulted from the frequency error between the synchronous clock and the not-yet-synchronized clock.

On that basis, Applicants submit that Hamada et al. does not identically disclose a phase error detecting circuit including all the limitations recited in independent claim 1. Specifically, the reference does not disclose, at a minimum, the following limitation:

> the reproduced data being data sampled and quantized by a not-yet-synchronized clock which is not yet adjusted to have a frequency of the synchronous clock, ...
>
> a phase error calculator... calculating... phase error data including a phase error amount resulted from a frequency error between the synchronous clock and the not-yet-synchronized clock; and
>
> a cross reference value generator for receiving the phase error data from the phase error calculator and updating the reference value of the cross detector based on the phase error data.

The claimed subject matter is configured for calculating the phase error data including **a phase error amount resulted from the frequency error between the synchronous clock and**

the not-yet-synchronized clock, and updating the reference value of the cross detector based on the phase error data, as claimed

By comparison, it is apparent, because of the above described differences, that Hamada does not disclose, among other things, that (1) the reproduction signal is data sampled by **the not-yet-synchronized clock**; (2) the phase error calculated by the phase error calculator includes **the phase error amount resulted from the frequency error between the synchronous clock and the not-yet-synchronized clock**; and (3) the reference value of the cross detector is updated based on the phase error amount. Accordingly, Applicants submit that Hamada et al. does not identically disclose a phase error detecting circuit including all the limitations recited in independent claim 1. Dependent claims 2-4 and 18 are also patentably distinguishable over Hamada et al. at least because these claims include all the limitations recited in independent claim 1. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims and favorable consideration thereof.

IV. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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